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REMARKS

Applicant acknowledges with appreciation the allowance of claims 26, 27, and 38, as well as the indication of allowability of claims 28-35, 37, 39, and 40. Claims 28, 33-37, 39, and 40 are amended to correct informalities. The specification is amended to correct informalities. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment.

The specification stands objected to because of informalities in the units of thickness and temperature used therein. The amendment to the specification overcomes this objection and it is respectfully requested to be withdrawn

Claims 28, 33-37, 39, and 40 stand objected to for informalities. The amendment to these claims overcomes the objection and it is respectfully requested to be withdrawn.

Claim 36 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 4,656,605 (Clayton) in view of U.S. patent 5,313,101 (Harada et al.). Applicant respectfully traverses this rejection.

Claim 36, as amended, defines a memory module with a memory circuit and recites, in part, "a titanium aluminide layer lining a bottom of the via hole" and "an aluminum plug on the titanium aluminide layer." This is not taught or suggested by Clayton or Harada et al. taken individually or in combination. Since the subject matter of claim 36 would not have been obvious over the references, the rejection of claim 36 over 35 U.S.C. § 103(a) is respectfully requested to be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: April 16, 2003

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Ryan H. Flax
Registration No.: 48,141
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant

Version With Markings to Show Changes Made

In the Specification:

At page 7, first full paragraph:

In this embodiment, a dual-layer lining comprised of a titanium aluminide layer 16 and a titanium nitride layer 17, in that sequence, is formed on the sidewalls and bottom of the via hole 200. The titanium aluminide layer 16 is preformed before the titanium nitride layer is deposited thereon. Exemplary techniques of this invention for preforming a titanium aluminide are described in greater detail in discussions set out below referencing FIGs. 2-4. To form the titanium nitride (TiN) layer 17, a reactive sputtering method can be used, in which the sputtering is effected in an ambient gas of N_2 + argon using a titanium target. The titanium nitride is deposited in a manner that provides complete coverage of the via hole sidewalls and the bottom of the via hole prelined with the titanium aluminide layer 16. A titanium nitride layer having a thickness of approximately 500-1000[Δ] Å generally is formed. The TiN layer 17 also could be deposited by other known techniques such as CVD. Also, the titanium nitride layer 17 could be replaced by a different type of titanium compound or other sufficiently conductive material that can be deposited as a thin film which provides comparable barrier functionality, such as a Ti-W thin film.

At page 8, first partial paragraph:

A refractory metal plug 14 is then deposited in the titanium aluminide/TiN-lined via hole 200. The refractory metal plug layer, such as tungsten, molybdenum, titanium, tantalum, or the like, can be deposited by CVD to conformally blanket coat the lined via hole and adjoining dielectric flats of the intermediate device structure. For instance, tungsten (W) can be deposited in the lined via hole 200 by conventional CVD methods using a hydrogen and/or silane hydrogen reduction of tungsten hexafluoride (WF_6) in which the premixed reactant gases are directed onto the surface of the

intermediate semiconductor structure having the lined via holes to be coated, which is maintained at an elevated temperature of approximately 440-450[E]°C for a process time that is sufficient to fill the lined via hole. When the mixed gases contact the substrate surface at the elevated temperature, the tungsten hexafluoride and the hydrogen (and/or silane) react to produce elemental tungsten (W), which is deposited upon onto the substrate as a film. A via or vertical interconnect structure has been formed at this juncture of the processing. The refractory metals can be used individually, as combinations thereof, or in combination with other low resistance materials to form the plug.

At page 9, first partial paragraph:

FIG. 2 shows an enlarged view of the via of FIG. 1 as fabricated according to a first embodiment of this invention. The via hole 200 is defined by a bottom 200' and sidewalls 200". The bottom 200' of the via hole 200 is the exposed surface of the underlying interconnection layer 12 until the via hole 200 is lined. The dielectric layers 11 and 13 and the ARC layer 18 are the same as described in connection with FIG. 1. Titanium aluminide 16 is directly sputter deposited on the via hole 200. To accomplish this, a titanium aluminide target is used in a sputtering chamber at approximately 2 kW dc target power at 1.5 mtorr pressure. When depositing titanium aluminide directly by sputtering, the titanium aluminide layer is formed at a thickness of approximately 100 to 700[Δ]Å, preferably about 400[Δ]Å, to provide the barrier properties desired of it.

At page 9, last partial paragraph, to page 10:

In one preferred implementation, the titanium aluminide layer 37 is formed by annealing at approximately 140 seconds at a 465[E] °C chuck temperature in a chamber. An approximately 50 to 300[Δ]Å titanium layer can deposited and the annealing is performed for a time sufficient such that the titanium at the bottom of the via hole 300 is substantially if not completely reacted with surface portions of the underlying aluminum conductor line 31 to form the titanium aluminide layer portion 37 at the bottom 300' of the via hole 300. The resulting titanium aluminide layer portion 37 can have a thickness of

approximately 100 to 700[Δ]Å, preferably about 400[Δ]Å, to provide the barrier properties desired of it. The titanium film deposited to line the sidewalls 300" and out of contact with aluminum of via hole 300 remains elemental titanium after the titanium aluminide formation.

At page 10, second full paragraph:

Experimentation has been performed which demonstrated and confirmed the barrier attributes possessed by the titanium aluminide layers formed according this invention. Specifically, 200[Δ]Å of Ti was deposited on top of 3.8 k[Δ]Å of Al formed on each of two separate Si wafers. A first Ti-coated wafer was heated in an anneal chamber to a temperature and for a time sufficient to form $TiAl_3$ by reaction of substantially all the Ti film with the contacted aluminum surface. The second Ti-coated wafer was not annealed. No TiN barrier layer was deposited over either test wafer. Then both wafers were subjected to fluorine attack in a CVD reactor chamber by exposure to WF_6 and heat of approximately 440[E]°C. This comparative test represented a worst case scenario by creating an environment comparable to cracking in a TiN barrier layer of where the TiN layer is discontinuous at the via bottom. As to the results of the experimentation, when viewed under high magnification, the first wafer having the $TiAl_3$ surface layer formed on the Al had no significant indications of fluorine attack. By contrast, the bare Ti-coated wafer suffered extensive fluorine attack seen as a dense cluster of island-like spots all across the surface of the Ti film. These results demonstrated that preformed titanium aluminide layers have high resistance to fluorine attack. Therefore, the preformed titanium aluminide layer formed in this invention provides a back-up measure of protection, in addition to the TiN barrier layer, against fluorine attack during fabrication of the vias.

In the Claims:

28. (Five Times Amended) A semiconductor memory device, comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the semiconductor substrate;

an antireflective coating over said first metallic layer;

a second dielectric layer over the antireflective coating;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the first metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole;

a second titanium aluminide layer or a titanium layer on sides of said via hole;

a titanium compound containing layer on the first titanium aluminide layer and in contact with said first titanium aluminide layer at an interface that is substantially free of tensile stress;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the conductive plug material.

33. (Five Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a first metallic layer over [a] the semiconductor substrate;

an antireflective coating over the first metallic layer;

a dielectric layer over the antireflective coating;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium layer lining sides of the via hole;

a titanium compound containing layer over the titanium aluminide layer and the titanium layer, said titanium compound layer being in contact with said titanium aluminide layer, wherein said titanium compound layer experiences approximately no tensile stress from said titanium aluminide layer;

a conductive plug material formed over the titanium compound layer;

a second metallic layer on the dielectric layer and electrically connected to the conductive plug material; and

a connector on the semiconductor substrate and wired to said memory circuit.

34. (Five Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a metallic layer over [a] the semiconductor substrate;

a dielectric layer over the metallic layer;

a via hole extending through the dielectric layer to a surface of the metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole;

a second titanium aluminide layer or a titanium layer lining sides of the via hole; and

a conductive material on the first titanium aluminide layer, wherein said conductive material and said first titanium aluminide layer are in contact at an interface having approximately no tensile stress from said first titanium aluminide layer; and

a connector on the semiconductor substrate and wired to said memory circuit.

35. (Five Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

an aluminum layer over [a] the semiconductor substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining a bottom of the via hole;

a titanium layer lining sides of the via hole;

a titanium nitride layer substantially free of through cracks on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the conductive plug material; and

a connector on the semiconductor substrate and wired to said memory circuit.

36. (Five Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a memory circuit region in [a] the semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer, said first metallic layer comprising aluminum;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer over the first metallic layer;

a via hole extending through the second dielectric layer to a surface of the first metallic layer;

a titanium aluminide layer lining a bottom of the via hole;

[a conductive] an aluminum plug [material] on the titanium aluminide layer [, said conductive plug material comprising aluminum]; and

a second metallic layer on the second dielectric layer and electrically connected to the aluminum plug material; and

a connector on the semiconductor substrate, said connector being wired to said memory circuit.

37. (Five Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a first metallic layer over a substrate;

a dielectric layer over the first metallic layer;

a via hole extending through the dielectric layer to a surface of the first metallic layer;

a titanium aluminide layer lining a bottom and sides of the via hole;

a titanium compound containing layer over the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer over the dielectric layer and electrically connected to the conductive plug material.

39. (Five Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

an aluminum layer over a substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining a bottom of the via hole;

a titanium layer lining sides of the via hole;

a titanium nitride layer substantially free of through cracks on the titanium aluminide layer and the titanium layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer and said titanium aluminide layer exerts approximately zero tensile stress upon said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the conductive plug material.

40. (Five Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer, said first metallic layer comprising aluminum;

a contact interconnect between the first metallic layer and the semiconductor substrate;

an antireflective coating over the first metallic layer;

a second dielectric layer over the antireflective coating;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the [second] first metallic layer;

a titanium aluminide layer lining a bottom and sides of the via hole;

a conductive plug material on the titanium aluminide layer, said conductive plug material comprising aluminum; and

a second metallic layer on the second dielectric layer and electrically connected to the conductive plug material, said second metallic layer comprising aluminum.